BANDGAP REFERENCE VOLTAGE GENERATOR

Field of the Invention

[0001] The present invention relates to electronics in general, and, more particularly, to a circuit for providing a bandgap voltage reference.

Background of the Invention

[0002] Applications for portable, battery-operated equipment or systems employing complex, high-performance electronic circuitry have increased with the widespread use of cellular telephones, laptop computers, and other systems. Maintaining the accuracy of many of these circuits is directly dependent on the stability of a reference voltage. A bandgap reference generator produces such a reference voltage. The reference voltage produced is approximately equal to the band gap voltage of silicon, which is approximately 1.2 volts. It is desirable that such a bandgap reference voltage be substantially immune to temperature variations, power supply variations, and noise.

[0003] Figure 1 depicts a schematic diagram of a bandgap reference architecture in the prior art. Power supply 101 feeds an unregulated (*i.e.*, fluctuating) signal to biasing network 103 and bandgap reference 105. Biasing network 103 provides a biasing signal via lead 115 to bandgap reference 105. Power supply 101, biasing network 103, and bandgap reference 105 are tied together via common lead 113, which is grounded. Bandgap reference 105 provides a reference signal, V_{out}, via lead 117.

[0004] Figure 2 depicts a schematic diagram of the same bandgap reference in the prior art as is depicted in Figure 1, but at the circuit (*i.e.,* lower) level of abstraction. M90 through M93 comprise a biasing network, the output of which, labeled 115, is fed to the gate of transistor M9. M9 acts as a current source for an error, or operational, amplifier comprising M9 through M13. The error amplifier senses the voltage levels at the gates of M10 and M11 and controls the currents through M5 and M6. The voltages at the gates of M10 and M11 are approximately equal due to the negative feedback of R1, R3, M5, and M6. Q1 through Q4 provide about twice the bandgap voltage of silicon, or 2.4 Volts. The bandgap transistors Q1 through Q4 also have canceling positive and negative temperature coefficients, so that the reference voltage output at 117, also the output of the error amplifier, is constant with temperature. Having two transistors cascaded as in Q1/Q2 or Q3/Q4 pairs reduces the offset voltage of the error amplifier, improving the accuracy of the

output voltage. If R1 = R3, the output voltage of the overall bandgap reference of the prior art can be expressed as:

$$V_{out} = V_{be(Q1)} + V_{be(Q2)} + 2*V_t*\ln(n)*(R2 + R3)/R3 \qquad \text{(Eq. 1)}$$

Where V_t is the threshold voltage of bipolar transistors (Q1 through Q4) and n is the emitter area ratio of Q1 and Q3. The emitter ratio of Q1/Q3 is equal to the emitter ratio of Q2/Q4 because Q1=Q2 and Q3=Q4.

[0005] Although this circuit is well known and widely used, it is disadvantageous in that it suffers from, among other things, a poor power supply rejection ratio (PSRR).

Summary of the Invention

[0006] The present invention provides a mechanism for improving the characteristics of a reference circuit, while avoiding many of the costs and restrictions associated with prior techniques. Specifically, embodiments of the present invention adds a self-biasing network to enable an improved power supply rejection ratio while maintaining temperature coefficient characteristics. The sub-circuits comprising the illustrative embodiment are a bandgap reference voltage generator, an operational amplifier, a transistor, a voltage divider, a startup network, and a self-biasing network.

[0007] An illustrative embodiment of the present invention comprises: a first transistor having a gate, a source, and a drain; a second transistor having a gate, a source, and a drain, wherein the gate of the second transistor is electrically connected to the gate of the first transistor, and wherein the source of the first transistor is electrically connected to the source of the second transistor; a first resistor having a first terminal and a second terminal, wherein the first terminal of the first resistor is electrically connected to the drain of the first transistor; a first capacitor having a first terminal and a second terminal, wherein the first terminal of the first capacitor is electrically connected to the drain of the first transistor; a second resistor having a first terminal and a second terminal, wherein the first terminal of the second resistor is electrically connected to the drain of the second transistor; and a second capacitor having a first terminal and a second terminal, wherein the first terminal of the second capacitor is electrically connected to the drain of the second transistor.

Brief Description of the Drawings

[0008] Figure 1 depicts a schematic diagram of a bandgap reference architecture in the prior art.

[0009] Figure 2 depicts a schematic diagram of a bandgap reference circuit in the prior art.

[0010] Figure 3 depicts a schematic diagram of a bandgap reference architecture in accordance with the illustrative embodiment of the present invention.

[0011] Figure 4 depicts a schematic diagram of a bandgap reference circuit in accordance with the illustrative embodiment of the present invention.

Detailed Description

[0012] Figure 3 depicts a schematic diagram of a bandgap reference architecture in accordance with the illustrative embodiment of the present invention. Power supply 301 feeds an unregulated signal in well-known fashion to bandgap reference 303, operational amplifier 305, transistor M35, and startup network 315 via lead 321.

[0013] Startup network 315 ensures an initial biasing voltage to pull the error amplifiers constituting bandgap reference 303 in working state. Startup network 315 does so by outputting a signal on lead 326 used by self-biasing network 311. Self-biasing network 311 takes the signal on lead 326 and outputs a biasing signal on lead 322 that is used by bandgap reference 303 and operational amplifier 305.

[0014] Bandgap reference 303 is a voltage generator. Bandgap reference 303 provides a reference signal via lead 324 to operational amplifier 305 by using input signals on leads 321 and 322. Operational amplifier 305 inputs the raw reference signal on lead 324, together with the signals on leads 321, 322, and 326, and outputs an amplified reference signal on lead 325.

[0015] Transistor M35 comprises a gate, a source, and a drain, and is a p-type metal oxide semiconductor (PMOS) device. The signal on lead 321 is fed into the source. The signal on lead 325 is fed into the gate. The drain of transistor M35 ties into lead 326.

[0016] Voltage divider 309 takes the signal on lead 326 and outputs the proper voltage reference signal on lead 328.

[0017] Power supply 301, bandgap reference 303, operational amplifier 305, voltage divider 309, and self-biasing network 311 are tied together via common lead 323, which is also tied to ground.

[0018] Figure 4 depicts a schematic diagram of the same bandgap reference, but at the circuit level, in accordance with the illustrative embodiment of the present invention. Power supply 301 comprises voltage source V1 with positive voltage applied to lead 321. Startup network 315 comprises transistors M60 and M61, interconnected as shown. The

signal on lead 321 is fed into the source of transistor M61. The drain of transistor M60 ties into lead 326.

[0019] Self-biasing network 311 comprises transistors M50 through M52 and capacitor C5, interconnected as shown. In self-biasing network 311, the voltage present on lead 328 is divided by three and provided via lead 322 to the tail transistors M9 and M30 of the error amplifiers within bandgap reference 303 and operational amplifier 305, respectively. By providing the reduced voltage, the dependence of the error amplifiers' biasing voltages on power supply 301 is reduced, consequently improving the power supply rejection ratio. At the same time, the temperature coefficient of the design is maintained. The source of transistor M52 is connected to lead 326. The gate of transistor M52 is connected to the drain of transistor M52. The source of transistor M51 is connected to the drain of transistor M52. The gate of transistor M51 is connected to the drain of transistor M51. The source of transistor M50 is connected to the drain of transistor M51. The gate of transistor M50 is connected to the drain of transistor M50. The drain of transistor M50 is connected to lead 323. Transistors M50 through M52 are PMOS devices. Capacitor C5 lies between leads 322 and 323.

[0020] Bandgap reference 303 comprises: transistors Q1 through Q4, transistors M9 through M13, transistors M5 and M6, resistors R1 through R3, and capacitors C1 and C2, interconnected as shown. Transistors M9 through M13 constitute the error amplifier within bandgap reference 303. The drain of transistor M9 is tied to lead 323. The sources of transistors M5, M6, M12, and M13 are tied to lead 321. The gates of transistors M5 and M6 are tied to each other. The drain of transistor M5 is tied to resistor R1 and capacitor C1. The drain of transistor M6 is tied to resistor R3 and capacitor C2 at lead 324. Capacitor C2 lies between leads 323 and 324.

[0021] In accordance with the illustrative embodiment, the value of resistor R1 equals the value of resistor R2, and the value of capacitor C1 equals the value of capacitor C2.

[0022] Operational amplifier 305 comprises transistors M30 through M34 operating as an error amplifier and capacitor C3, interconnected as shown. The bias signal on lead 322 is fed into transistor M30. The drain of transistor M30 is tied to lead 323. The signal on lead 321 is fed into the sources of transistors M33 and M34. The signal on lead 324 as provided by bandgap reference 303 is fed into the gate of transistor M32. The drain of transistor M34 is tied to lead 325. Capacitor C3 lies between lead 323 and 326.

[0023] Voltage divider 309 comprises transistors M40 through M43 and capacitor C4, interconnected as shown. Voltage divider 309 provides reference signal V_{out} on lead 328 at a voltage level that is three-fourths of the voltage level present on lead 326.

[0024] Capacitors C1 through C5 further assist in damping the effect of power supply variation the signal on lead 324.

[0025] The output voltage of the illustrative embodiment, V_{out}, is equal to:

$$V_{out} = \frac{3\left[V_{be}(Q_1) + V_{be}(Q2) + 2V_t \ln(n)\left(\frac{R_2 + R_3}{R_3}\right)\right]}{4} \qquad \text{(Eq. 2)}$$

wherein $V_{be}(Q_1)$ is the base-emitter voltage in transistor Q_1, $V_{be}(Q_2)$ is the base-emitter voltage in transistor Q_2, V_t is the threshold voltage of Where V_t is the threshold voltage of bipolar transistors (Q1 through Q4) and n is the emitter area ratio of Q1 and Q3. The emitter ratio of Q1/Q3 is equal to the emitter ratio of Q2/Q4 because Q1=Q2 and Q3=Q4.

[0026] It is to be understood that the above-described embodiments are merely illustrative of the present invention and that many variations of the above-described embodiments can be devised by those skilled in the art without departing from the scope of the invention. It is therefore intended that such variations be included within the scope of the following claims and their equivalents.

[0027] What is claimed is: